

DLV11

DIAGNOSTIC TEST
MD-11-DVKAE-B

EP-DVKAE-B-DL-A
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The microfiche card contains a grid of frames on the left side, organized into three columns. The first column contains 12 frames, the second column contains 12 frames, and the third column contains 12 frames. Each frame contains data, including text and numerical values. The data is organized into tables with multiple rows and columns. The text is small and difficult to read, but it appears to be technical data. The right side of the card is a large, dark, rectangular area, likely a placeholder for a larger image or a blank space for notes.

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DVKAE-B-D
PRODUCT NAME: DLV11 TEST
DATE: OCTOBER 1976
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: R.D. FIORENTINO
REVISION B: D.J. CASALETTO

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1. ABSTRACT

THIS IS A LOGIC TEST OF THE DLV11 SERIAL LINE UNIT FOR
THE LSI-11 COMPUTER. THIS TEST WILL OPERATE ON
THE DLV11 WITHOUT ANY SPECIAL TEST DEVICES BY DEFAULT.
HOWEVER, A SPECIAL WRAP MODULE CAN BE USED AND TESTED
BY OPTION.

THIS IS A MULTIPLE DEVICE TEST WHICH WILL OPERATE ON THE
CONSOLE DLV11 ADDRESSED AT 177560, AND UP TO 8 ADDITIONAL

DLV11'S WITH SPECIFIED ADDRESSES.

DEFAULT ADDRESSES FOR MULTIPLE DEVICE TESTING ARE:

177550
176500

CONSOLE

BASE ADDRESS FOR ADDITIONAL DLV11'S

FOR COMPLETE INSTRUCTIONS ON MULTIPLE DEVICE TESTING SEE
SECTION 5.5

2. REQUIREMENTS

2.1 EQUIPMENT

LSI-11 COMPUTER
DLV11 SERIAL LINE UNIT
TERMINAL FOR DLV11
TEST MODULE (BY OPTION)

2.2 STORAGE REQUIREMENTS

4K MEMORY

3. LOADING PROCEDURE

3.1 METHOD

ABSOLUTE LOADER

4. STARTING PROCEDURE

200 - NORMAL ENTRY

TO LOAD AND EXECUTE

1. LOAD PROGRAM WITH THE ABSOLUTE LOADER.
2. IF ANY PROGRAM OPTIONS ARE REQUIRED, SET THE APPROPRIATE BIT IN THE SOFTWARE SWITCH REGISTER AT LOCATION 122. (REF. SECTION 5.1)
3. START PROGRAM AT 200.
4. PROGRAM WILL PRINT "END OF PASS" FOLLOWING EACH PASS.
TO LOAD AND EXECUTE

STARTING ADDRESS:

200 - NORMAL ENTRY

4.1 CONTROL SWITCH SETTING

THIS PROGRAM CONTAINS A SOFTWARE SWITCH REGISTER FOR OPTION SELECTION (LOC 422). FOR IT TO OPERATE THE OPERATOR MUST SELECT THE APPROPRIATE OPTION BY SETTING OR RESETTING THE RESPECTIVE BIT IN THE WORD.

TO DO THIS, THE LSI-11 MUST BE IN ODT MODE.

4.2 EXECUTION TIME

AT 110 BAUD, EXECUTION TIME FOR A SINGLE DEVICE IS APPROXIMATELY 30 SECONDS. FOR HIGHER BAUD RATES, EXECUTION TIME MUST BE REDUCED BY AN APPROPRIATE FACTOR.

5. GENERAL OPERATING PROCEDURE.

1. THE PROGRAM WILL CYCLE CONTINUOUSLY UNLESS HALTED BY THE OPERATOR, OR SOME ERROR CONDITION.
2. TO HALT THE PROGRAM, DEPRESS THE BREAK KEY. ODT WILL DISPLAY THE PC AT WHICH IT WAS HALTED.
3. IF NEW OPTIONS ARE TO BE SELECTED IN THE SMR, THEY MUST BE SET AT THIS TIME.
4. CONTINUE THE PROGRAM VIA A "P" OR A "G" COMMAND.

5.1 SOFTWARE SWITCH SETTINGS

BIT15 - CONTINUE ON ERROR	(100000)
BIT14 - LOOP ON CURRENT ERROR	(040000)
BIT13 - NOT USED	(020000)
BIT12 - NOT USED	(010000)
BIT11 - NOT USED	(004000)
BIT10 - LOOP ON CURRENT TEST	(002000)
BIT9 - RUN WRAP TEST	(001000)
BIT8 - SET DEVICE MAP MANUALLY	(000400)
BIT7 - NOT USED	(000200)
BIT6 - NOT USED	(000100)
BIT5 - NOT USED	(000040)
BIT4 - NOT USED	(000020)
BIT3 - NOT USED	(000010)
BIT2 - NOT USED	(000004)
BIT1 - NOT USED	(000002)
BIT0 - NOT USED	(000001)

5.2 SLU CONFIGURATION REQUIREMENTS

FOR BAUD RATE	#STOP BITS	#BITS
110	2	8
ALL OTHERS	1	8

NO OTHER CONFIGURATION IS TESTED BY THIS PROGRAM
EIA IS TESTED WITH THE WRAP MODULE OPTION TEST.

5.3 OPERATION UNDER APT

THIS PROGRAM WILL OPERATE UNDER APT WITHOUT MODIFICATION TO THE SMR. HOWEVER, IN ORDER TO TEST THE FULL CAPABILITY OF THE DLV11, A TEST WITH THE TEST MODULE IS NECESSARY.
TO DO THIS, APT MUST SET BIT9 IN THE SWITCH REGISTER PRIOR TO EXECUTION.

IMPORTANT ::::: THE TEST TIMES, PASS TIME CONSTANTS WITHIN
THIS PROGRAM REFLECT OPERATION AT 9600 BAUD.
A SLOWER BAUD RATE WILL CAUSE APT TO ABORT TESTING

5.4 TESTING A DLV11 AT A UNIQUE ADDRESS

1. TO SPECIFY A CONSOLE ADDRESS OTHER THAN 177560 OR VECTOR 60, THE OPERATOR MUST SUPPLY THE PROGRAM WITH THE CORRECT ADDRESSES BY INSERTING THEM AT THE TAG LABELED "RCSR". THE ADDRESSES MUST BE IN THE FOLLOWING ORDER:

RCSR:	ADDRESS OF RECEIVER CSR
RBUF:	ADDRESS OF RECEIVER BUFFER
TCSR:	ADDRESS OF TRANSMITTER CSR
TBUF:	ADDRESS OF TRANSMITTER BUFFER
RVECT:	ADDRESS OF RECEIVER VECTOR
RPSW:	ADDRESS OF ASSOCIATED PSW
TVECT:	ADDRESS OF TRANSMITTER VECTOR
TPSW:	ADDRESS OF ASSOCIATED PSW

2. TO TEST A SINGLE DLV11 AT A UNIQUE ADDRESS, INSERT THE ADDRESS OF THE RECEIVER CSR IN LOCATION SBASE, AND THE ADDRESS OF THE VECTOR IN LOCATION SVECT1, IN THE ETABLE. THE PROGRAM WILL GENERATE THE ADDITIONAL CSR, BUFFER, AND VECTOR ADDRESSES NEEDED FOR TESTING.

5.5 TESTING MULTIPLE DLV11 MODULES

ADDITIONAL DLV11'S MUST BE ADDRESSED WITHIN A RANGE OF 8 SEQUENTIAL ADDRESSES. A BASE ADDRESS MAY BE SPECIFIED BY THE OPERATOR OR A DEFAULT ADDRESS OF 176500 AND DEFAULT VECTOR OF 300 ARE USED. THE PROGRAM GENERATES A TABLE OF 8 ADDRESSES WITH EACH CSR GIVEN IN INCREMENTS OF 10. THE PROGRAM WILL THEN SIZE FOR DEVICES PRESENT.

5.6 THE DEVICE MAP

WHEN THE PROGRAM SIZES, A DEVICE MAP IS ESTABLISHED TO REPRESENT THOSE DEVICES PRESENT AND THEIR CORRESPONDING RECEIVER CSR ADDRESSES. THE DEVICE MAP CAN ALSO BE SET BY THE OPERATOR BY SELECTING THE APPROPRIATE BIT IN THE SWITCH REGISTER (SEE SECTION 5.1) AND PROCEEDING AS INDICATED BELOW.

THE DEVICE MAP IS A 16 BIT WORD WITH BITS 0-8 ARRANGED AS FOLLOWS:

8	7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---	---

DEVICE #0 = CONSOLE DEFAULT ADDRESS = 177560; VECTOR = 60
DEVICES #1-#8 = ADDITIONAL DLV11'S
DEVICE #1 = BASE ADDRESS (SBASE); BASE VECTOR (SVECT1)
DEVICE #2 = BASE ADDRESS + 10; BASE VECTOR + 10

DEVICE 83 = BASE ADDRESS + 20; BASE VECTOR + 20
 DEVICE 84 = BASE ADDRESS + 40; BASE VECTOR + 40
 DEVICE 85 = BASE ADDRESS + 60; BASE VECTOR + 60
 DEVICE 86 = BASE ADDRESS + 80; BASE VECTOR + 80
 DEVICE 87 = BASE ADDRESS + 100; BASE VECTOR + 100
 DEVICE 88 = BASE ADDRESS + 120; BASE VECTOR + 120

SETTING THE APPROPRIATE BITS IN THE DEVICE MAP
 (DEVN LOC 456) WILL DESIGNATE THOSE DEVICES WHICH
 ARE TO BE TESTED. THE PROGRAM IS STARTED AS USUAL,
 BUT WILL COME TO A PROGRAMMED HALT TO ALLOW THE OPERATOR
 TO LOAD THE DEVICE MAP WHILE IN ODT MODE. A
 "P" COMMAND WILL RESUME EXECUTION OF THE PROGRAM.

6. ERRORS

ALL ERROR REPORTS WITHIN THIS TEST ARE IN THE FORM
 OF AN ERROR HALT. ON THE LSI-11, A HALT WILL FORCE
 ODT TO DISPLAY THE PC+2 OF THE HALT. THIS IS
 THE PRIMARY ERROR INDICATOR WITHIN THE PROGRAM.
 UPON DETECTION OF AN ERROR, THE PROGRAM WILL PLACE THE
 CURRENT ERROR NUMBER AND THE CURRENT TEST IN THE MAILBOX
 (SEE IMPORTANT TAGS SEC. 7.1)
 TO DETERMINE THE TYPE OF ERROR, THE OPERATOR MUST REFER-
 ENCE THE LISTING.

6.1 ERROR ISOLATION

TO DETERMINE WHICH DEVICE FAILED IN A MULTIPLE TEST
 ENVIRONMENT, CHECK THE RECEIVER CSR ADDRESS AT
 LOCATION 506. THE UNIT NUMBER CAN ALSO BE USED TO
 LOCATE THE DEFECTIVE DLV11. THIS LOCATION KEEPS
 TRACK OF THE DEVICE # UNDER TEST. (SEE SECTION 5.6
 FOR ADDRESS OF THAT DEVICE).

6.1 ERROR RECOVERY

IN ORDER TO CONTINUE, THE OPERATOR MUST ISSUE A "P" TO
 CONTINUE THE PROGRAM, OR MAY SET THE ERROR LOOP SWITCH
 PRIOR TO CONTINUING.

7.0 MISCELLANEOUS

7.1 IMPORTANT TAGS

FOLLOWING IS A LIST OF IMPORTANT TAGS WITHIN THE LISTING

TAG	COMMENT
SMAIL	START OF THE PROGRAM MAILBOX. MANY CLUES TO PROBLEMS CAN BE FOUND HERE
SFATAL	ERROR NUMBER. USE THE TABLE OF CONTENTS TO LOCATE THE ERROR INFORMATION AND/OR CODE

[illegible]

STESTN	CURRENT TEST NUMBER
SPASS	PASS COUNT OF THE PROGRAM WHEN ERROR WAS DETECTED OR PROGRAM HALTED
SSWREG	SOFTWARE SWITCH REGISTER
RCSR	ADDRESS OF RECEIVER CSR UNDER TEST
RBUF	ADDRESS OF RECEIVER BUFFER UNDER TEST
TCSR	ADDRESS OF TRANSMITTER CSR UNDER TEST
TBUF	ADDRESS OF TRANSMITTER BUFFER UNDER TEST
RVECT	RECEIVER VECTOR ADDRESS BEING USED
TVECT	TRANSMITTER VECTOR ADDRESS BEING USED

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REVISION

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8
IN TST12, FILLED SECOND BUFFER & CHECKED FOR
"DONE" CLEAR BEFORE FLAGGING AN ERROR
REMOVED TEST THAT CHECKED "RESET" SETS "DONE"
ON TRANSMITTER. (RESET DOES NOT SET DONE)
ADDED MULTIPLE SLU TEST CAPABILITY
CHANGED PROGRAM TO SKIP TST17 UNDER APT WHEN TESTING
THE CONSOLE AFTER THE FIRST PASS

[illegible]

```

000000 000000 .ENABL ABS
000002 000002 .MLIST MC,CND,MD
000004 000000 .LIST ME
000006 000006 .=0
000010 000012 .+2 ;UNASSIGNED TRAP
000012 000000 .0
000014 000016 .+2 ;TIME-OUT, BUS ERROR
000016 000000 .0
000020 000022 .+2 ;RESERVED INSTRUCTION
000022 000000 .0
000030 000030 .=30
000032 000032 .+2 ;ENT TRAP
000034 000036 .0
000036 000000 .+2
000040 000042 .0
000042 000000 .+2
000046 000046 .=46
000050 000050 .+2
000052 000054 .0
000054 000000 .+2
000056 000060 .0
000060 000000 .+2
000062 000064 .0
000064 000000 .+2
000066 000070 .0
000070 000000 .+2
000072 000074 .0
000074 000000 .+2
000100 000100 .NCALL .STYPE,.STRAP,.SAPTBL,.SAPTHDR,.SAPTYPE,STARS
000102 000102 .=100
000102 000002 .102
000200 000200 .RTI
000200 012737 005426 000024 .=200
000206 012737 000340 000026 .NOV #PWRFL,3824 ;SET POWER FAIL VECTOR
000214 005067 000166 .NOV #340,3826 ;SET POWER FAIL PSW
000220 005067 000156 .CLR SPASS ;CLEAR PASS COUNT
000224 005067 000154 .CLR SFATAL ;STARTING POINT AFTER POWER FAIL
000230 005067 000154 .CLR $TESTN ;CLEAR TEST NUMBER
000234 005067 000152 .CLR $DEVCT ;CLEAR DEVICE COUNT
000240 004767 005062 .CLR $UNIT ;SET UNIT NUMBER TO ZERO
000244 005500 .JSR PC,MSGPRT ;PRINT PROGRAM NAME
000246 000167 000726 .WORD M1
000400 000400 .JMP START ;START DIAGNOSTIC
000400 000400 .=400
.SBTTL APT MAILBOX-ETABLE
;*****
.EVEN

```

370	000400	
371	000400	000000
372	000402	000000
373	000404	000000
374	000406	000000
375	000410	000000
376	000412	000000
377	000414	000000
378	000416	000000
379	000420	
380	000420	000
381	000421	000
382	000422	000000
383	000424	000000
384	000426	000000
385		
386		
387		
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389		
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391	000430	000
392	000431	000
393		
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396		
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398	000432	000000
399		
400	000434	000
401	000435	000
402	000436	000000
403	000440	000
404	000441	000
405	000442	000000
406	000444	000
407	000445	000
408	000446	000000
409	000450	000300
410	000452	000000
411	000454	176500
412	000456	000000
413	000460	

SMAIL:		
SMISGTY:	.WORD	AMISGTY
SFATAL:	.WORD	AFATAL
STESTN:	.WORD	ATESTN
SPASS:	.WORD	APASS
SDEVCT:	.WORD	ADEVCT
SUNIT:	.WORD	AUNIT
SMSGAD:	.WORD	AMSGAD
SMSGLG:	.WORD	AMSGLG
SETABLE:		
SENV:	.BYTE	AENV
SENMH:	.BYTE	AENMH
SSUREG:	.WORD	ASUREG
SUSMR:	.WORD	AUSMR
SCPUOP:	.WORD	ACPUOP
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SHANS1:	.BYTE	AHANS1
SHNTP1:	.BYTE	AHNTP1
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SHADR1:	.WORD	AHADR1
.		
SHANS2:	.BYTE	AHANS2
SHNTP2:	.BYTE	AHNTP2
SHADR2:	.WORD	AHADR2
SHANS3:	.BYTE	AHANS3
SHNTP3:	.BYTE	AHNTP3
SHADR3:	.WORD	AHADR3
SHANS4:	.BYTE	AHANS4
SHNTP4:	.BYTE	AHNTP4
SHADR4:	.WORD	AHADR4
SVECT1:	.WORD	AVECT1
SVECT2:	.WORD	AVECT2
SBASE:	.WORD	ABASE
SDEVH:	.WORD	ADEVH
SETEND:		
NEXTT		

```

::: APT MAILBOX
::: MESSAGE TYPE CODE
::: FATAL ERROR NUMBER
::: TEST NUMBER
::: PASS COUNT
::: DEVICE COUNT
::: I/O UNIT NUMBER
::: MESSAGE ADDRESS
::: MESSAGE LENGTH
::: APT ENVIRONMENT TABLE
::: ENVIRONMENT BYTE
::: ENVIRONMENT MODE BITS
::: APT SWITCH REGISTER
::: USER SWITCHES
::: CPU TYPE, OPTIONS
BITS 15-11=CPU TYPE
      11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
      11/70=06, PD0=07, 0=10
BIT 10=REAL TIME CLOCK
BIT 9=FLOATING POINT PROCESSOR
BIT 8=MEMORY MANAGEMENT
::: HIGH ADDRESS, H.S. BYTE
::: MEM. TYPE, BLK#1
MEM. TYPE BYTE -- (HIGH BYTE)
      900 NSEC CORE=001
      300 NSEC BIPOLAR=002
      500 NSEC MOS=003
::: HIGH ADDRESS, BLK#1
MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
::: HIGH ADDRESS, H.S. BYTE
::: MEM. TYPE, BLK#2
MEM. LAST ADDRESS, BLK#2
::: HIGH ADDRESS, H.S. BYTE
::: MEM. TYPE, BLK#3
MEM. LAST ADDRESS, BLK#3
::: HIGH ADDRESS, H.S. BYTE
::: MEM. TYPE, BLK#4
MEM. LAST ADDRESS, BLK#4
::: INTERRUPT VECTOR#1, BUS PRIORITY#1
::: INTERRUPT VECTOR#2, BUS PRIORITY#2
::: BASE ADDRESS OF EQUIPMENT UNDER TEST
::: DEVICE MAP

```

.SBTTL APT PARAMETER BLOCK

```

*****
;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
*****
      .SX=.      :SAVE CURRENT LOCATION
      .Z24      :SET POWER FAIL TO POINT TO START OF PROGRAM
      200       :FOR APT START UP
      .Z44      :POINT TO APT INDIRECT ADDRESS PNTR.
      $APTHDR    :POINT TO APT HEADER BLOCK
      .Z.SX      :RESET LOCATION COUNTER
*****
;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
;INTERFACE SPEC.

```

```

$APTHD:
SHIFTS: .WORD 0      ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
$MBADR: .WORD $MAIL   ;; ADDRESS OF APT MAILBOX (BITS 0-15)
$TSTH:  .WORD 10     ;; RUN TIM OF LONGEST TEST
$PASTH: .WORD 10     ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
$UNITH: .WORD 0      ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
      .WORD SETEND-$MAIL/2 ;; LENGTH MAILBOX-ETABLE(WORDS)

```

EQUATES

```

X=1
N=1
AVECT1=300
ABASE=176500
STKPTH=1000
CSR=177560
BIT15=100000
BIT14=40000
BIT13=20000
BIT12=10000
BIT11=4000
BIT10=2000
BIT9=1000
BIT8=400
BIT7=200
BIT6=100
BIT5=40
BIT4=20
BIT3=10
BIT2=4
BIT1=2
BIT0=1

```

```

;DEFAULT BASE VECTOR FOR ADDITIONAL UNITS
;DEFAULT BASE DEVICE ADDRESS FOR ADDITIONAL UNITS
;DEFAULT CONSOLE DEVICE ADDRESS

```

414
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416
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500

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000460
000024
000024
000044
000460
000460
000460
000460
000000
000460
000400
000460
000010
000460
000010
000470
000000
000472
000030

```

```

000001
000001
000300
176500
001000
177560
100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

```


K01

.MAIN. MACY11 27(732) 04-OCT-76 14:23 PAGE 11
DVKAEB.P11 APT PARAMETER BLOCK

461 000474 000000
462 000476 000000
463 000500 000000
464 000502 000000
465 000504 000000
466
467
468

TMP0: .WORD 0
TMP1: .WORD 0
TMP2: .WORD 0
TMP3: .WORD 0
CTSTFL: .WORD 0

:LOCATION TO STORE TABLE OFFSETS
:LOCATION TO KEEP NO. OF TEST DEVICES
:LOCATION TO KEEP DEVICE MAP TEST MASK
:FLAG TO INDICATE CURRENT TEST DEVICE IS CONSOLE

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489
490
491
492
493

000506	177560
000510	177562
000512	177564
000514	177566
000516	000060
000520	000062
000522	000064
000524	000066
000526	177560
000530	177562
000532	177564
000534	177566
000536	000060
000540	000062
000542	000064
000544	000066
	000600
000600	000020
000640	000010

REGISTER AND VECTOR ADDRESSES FOR THE DLV11 UNDER TEST

```

RCSR:  C5R
RBUF:  C5R+
TCSR:  C5R+
TBUF:  C5R+
RVECT: 60
RPSM:  62
TVECT: 64
TPSM:  66

```

! INITIAL REGISTER AND VECTOR ADDRESSES FOR THE CONSOLE DLV11

DRCSR:	177560	:ADDRESS OF RECEIVER STATUS REGISTER
DRBUF:	177562	:ADDRESS OF RECEIVER DATA BUFFER REGISTER
DTCSR:	177564	:ADDRESS OF TRANSMITTER STATUS REGISTER
DTBUF:	177566	:ADDRESS OF TRANSMITTER DATA BUFFER REGISTER
DRVECT:	60	
DRPSN:	62	
DTVECT:	64	
DTPSN:	66	

AORTBL: .#600 20
VCTTBL: .BLKH 10

```

491 001200 001200 001000 START: MOV #1200 ; INITIALIZE STACK POINTER
492 001200 012706 001000 ; ROUTINE TO HANDLE THE TESTING OF MULTIPLE DLV11 MODULES
493 001204 005767 177176 TST SPASS ; CHECK IF ON FIRST PASS
494 001210 001161 BNE SIZED ; IF NOT ON FIRST PASS
495 001212 132767 000001 177200 BITB #BIT0,SENV ; CHECK IF ON APT
496 001220 001404 BEQ MANL ; IF NOT ON APT
497 001222 132767 000200 177171 BITB #BIT7,SENVH ; DID APT SIZE?
498 001230 001067 BNE APTSIZ ; IF APT SIZED
499 001232 032767 000400 177162 MANL: BIT #BIT8,SSWREG ; MANUAL SETTING OF SDEVH?
500 001240 001402 BEQ SETTBL ; NO
501 001242 000000 HALT ; INPUT DEVICE MAP
502 001244 000461 BR APTSIZ ; CONT WHEN DEVICE MAP IS SET
503 001246 004767 000104 SETTBL: JSR PC,DEVADR ; GENERATE DEVICE ADDRESS TABLE
504 001252 005067 177222 CLR TMP2 ; CLEAR TEMP LOCATION TO COUNT DEVICES
505 001254 005067 177174 CLR SDEVH ; CLEAR DEVICE MAP
506 001256 012737 001316 000004 MOV #25,2#4 ; SET TIMEOUT POINTER
507 001258 016700 177160 MOV SBASE,R0 ; LOAD BASE ADDRESS
508 001260 062700 000100 ADD #100,R0 ; POINT R0 TO UNIT#8 (UNIT#0 = CONSOLE)
509 001262 162700 000010 1S: SUB #10,R0 ; POINT R0 TO THE NEXT UNIT ADDRESS
510 001264 005710 TST (R0) ; CHECK FOR DEVICE EXISTANCE
511 001266 005267 177144 INC SDEVH ; NO TIMEOUT - INDICATE DEVICE IN DEVICE MAP
512 001268 005267 177162 INC TMP2 ; INCREMENT DEVICE COUNT
513 001270 006382 177134 2S: ASL SDEVH ; ADJUST DEVICE MAP FOR NEXT UNIT CHECK
514 001272 026700 177126 CHP SBASE,R0 ; FINISHED SIZING?
515 001274 002764 BLT 1S ; BR IF NOT
516 001276 016700 177172 MOV DCRSR,R0 ; LOAD CONSOLE DEVICE ADDRESS
517 001278 012737 001354 000004 MOV #35,2#4 ; SET TIMEOUT VECTOR
518 001280 005710 TST (R0) ; TEST FOR CONSOLE EXISTANCE
519 001282 005267 177106 INC SDEVH ; NO TIMEOUT - INDICATE CONSOLE IN DEVICE MAP
520 001284 005267 177124 INC TMP2 ; INCREMENT DEVICE COUNT
521 001286 000432 3S: BR VCTADR ; BR TO GENERATE VECTOR ADDRESS TABLE

; ROUTINE TO GENERATE DEVICE ADDRESS TABLE
522 001356 012702 000600 DEVADR: MOV #AORTBL,R2 ; POINT R2 TO TOP OF THE ADDRESS TABLE
523 001358 016700 177066 MOV SBASE,R0 ; LOAD BASE ADDRESS IN R0
524 001360 010001 MOV R0,R1 ; CALCULATE DEVICE ADDRESS LIMIT
525 001362 062701 000100 ADD #100,R1
526 001364 010022 1S: MOV R0,(R2)+ ; MOVE DEVICE ADDRESS TO TABLE
527 001366 062700 000010 ADD #10,R0 ; CALCULATE NEXT DEVICE ADDRESS
528 001368 020001 CHP R0,R1 ; FINISHED?
529 001370 002773 BLT 1S ; BR IF NOT
530 001372 000207 RTS PC ; RETURN

531 001410 005067 177064 APTSIZ: CLR TMP2 ; CLEAR TEMP LOCATION TO KEEP DEVICE COUNT
532 001412 016702 177036 MOV SDEVH,R2 ; GET DEVICE MAP
533 001414 005702 TSTDVH: TST R2 ; TEST MSB OF DEVICE MAP
534 001416 100002 BPL 1S ; BR, IF CLEAR
535 001418 005267 177060 INC TMP2 ; IF SET, INCREMENT DEVICE COUNT
536 001420 006302 ASL R2 ; SHIFT NEXT BIT INTO MSB POSITION
537 001422 001401 DCRDT ; FINISHED (NO BITS LEFT SET IN MAP)?
538 001424 000771 BR TSTDVH ; BR, IF NOT

```

001436	004767	177714	DVADT:	JSR	PC,DEVADR	;GENERATE DEVICE ADDRESS TABLE
001442	012702	000640	VCTADR:	MOV	#VCTTBL,R2	;GET LOCATION OF VECTOR TABLE
001446	005001			CLR	R1	;CLEAR DATA WORD
001450	116700	176774		MOV	\$VECT1,R0	;COPY BASE VECTOR
001454	042700	177400		BIC	#177400,R0	;CLEAR BYTE SIGN EXTENSION
001460	010022		IS:	MOV	R0,(R2)+	;PUT VECTOR ADDRESS IN THE TABLE
001462	005201			INC	R1	;KEEP COUNT OF THE NO. OF ADDRESSES STORED
001464	062700	000010		ADD	#10,R0	;FORM NEXT SEQUENTIAL ADDRESS
001470	022701	000010		CMF	#10,R1	;FINISHED?
001474	002371			BGE	IS	;IF NO
001476	016700	176776		MOV	TMP2,R0	;COPY DEVICE COUNT INTO R0
001502	005001			CLR	R1	;CLEAR AUXILIARY REGISTER
001504	000300			SHAB	R0	;PUT DEVICE COUNT IN UPPER BYTE OF R0
001506	006300			ASL	R0	;MOVE MSB OF COUNT INTO
001510	006300			ASL	R0	;MSB OF R0
001512	006300		SHIFT:	ASL	R0	;PUT MSB OF COUNT INTO CARRY
001514	106101			ROLB	R1	;MOVE MSB OF COUNT INTO R1
001516	006300			ASL	R0	;MOVE NEXT BIT OF COUNT
001520	106101			ROLB	R1	;INTO R1
001522	006300			ASL	R0	;MOVE LAST BIT OF DIGIT
001524	106101			ROLB	R1	;INTO R1
001526	062701	000060		ADD	#60,R1	;CONVERT TO ASCII
001528	000301			SHAB	R1	;MOVE DIGIT TO UPPER BYTE
001530	032701	000020		BIT	#BIT4,R1	;HAVE BOTH DIGITS BEEN MOVED TO R1?
001532	001764			BEG	SHIFT	;BR, IF NOT
001534	010167	003774		MOV	R1,R2	;MOVE DEVICE COUNT TO OUTPUT MESSAGE
001536	004767	003554		JSR	PC,HSGPRT	;PRINT MESSAGE DEFINING THE
001538	005542			WORD	R2	;NO. OF DEVICES SIZED
001540	005067	176716	SIZED:	CLR	TMP1	;CLEAR TEMP LOCATION FOR TABLE OFFSETS
001542	012767	000002		MOV	#BIT1,TMP3	;SET UP BIT MASK FOR DEVICE MAP
001544	032767	000001	176714	BIT	#BIT0,\$DEVH	;IS CONSOLE DEVICE TO BE TESTED?
001546	001001		176662	BNE	TCONSL	;IF YES
001548	000414			BR	SETUP	;GO TEST ADDITIONAL DEVICES
001550	012700	000506		MOV	#RCSR,R0	;SET UP REGISTER ADDRESSES FOR CONSOLE
001552	012701	000526		MOV	#RCSR,R1	;POINT R1 TO CONSOLE ADDRESS TABLE
001554	005267	176670		INC	CTSTFL	;INDICATE THAT CONSOLE IS UNDER TEST
001556	012120		IS:	MOV	(R1)+,(R0)+	;FORM CONSOLE ADDRESSES
001558	022700	000524		CMF	#TPSH,R0	;FINISHED?
001560	002374			BGE	IS	;IF NO
001562	000167	000116		JMP	TST1	;GO TEST CONSOLE DEVICE
001630	036767	176646	176620	SETUP:	BIT	TMP3,\$DEVH
001636	001010			BNE	SETADR	;TEST DEVICE BIT IN DEVICE MAP
001640	006367	176636		ASL	TMP3	;BR, IF SET AND TEST DEVICE
001644	062767	000002	176624	ADD	#2,TMP1	;IF CLEAR, UPDATE DEVICE MAP TEST MASK
001652	005267	176534		INC	\$UNIT	;INCREMENT TABLE OFFSET
001656	000764			BR	SETUP	;INCREMENT UNIT NUMBER
001660	005267	176526		SETADR:	INC	\$UNIT
001664	006367	176612		ASL	TMP3	;BR, TO TEST NEXT DEVICE MAP BIT
001670	016702	176602		MOV	TMP1,R2	;INCREMENT UNIT NUMBER BEFORE TESTING DEVICE
001674	062767	000002	176574	ADD	#2,TMP1	;UPDATE DEVICE MAP TEST MASK
						;UPDATE TABLE OFFSET FOR NEXT DEVICE


```

001702 011200 000600      MOV      AORTBL(R2),R0      ; REGISTER ADDRESS OF NEXT DEVICE
001706 012701 000506      MOV      @RCSR,R1      ; LOCATION OF REGISTER ADDR.
ADR:    001712 010021      MOV      R0,(R1)+      ; CREATE ACTIVE DEVICE ADDRESS TABLE
        001714 005720      TST       (R0)+
        001716 030027 000006      BIT      R0,#000006      ; FINISHED?
        001722 001373      BNE      ADR          ; BR, IF NOT

001724 011200 000640      MOV      VCTTBL(R2),R0      ; VECTOR ADDRESS OF NEXT DEVICE
VECT:   001730 010021      MOV      R0,(R1)+      ; CREATE ACTIVE VECTOR ADDRESS TABLE
        001732 005720      TST       (R0)+
        001734 030027 000006      BIT      R0,#000006      ; FINISHED?
        001740 001373      BNE      VECT         ; BR, IF NOT
        001742 000167 000000      JNP      TST1      ; GO TEST THIS DEVICE

; TEST ABILITY TO REFERENCE RECEIVER CSR WITHOUT TRAPPING
TST1:   001746 012767 000001 176430      MOV      #1,STESTN      ; MOVE TEST NUMBER TO MAILBOX
        001754 012737 001770 000004      LP1:    MOV      #25,204 ; SET TIME OUT VECTOR
        001762 005777 176520      TST      @RCSR      ; REFERENCE THE CSR
        001766 000416      BR        IS          ; GO TO NEXT TEST IF NO TRAP

        001770 032767 040000 176424      ZS:     BIT      @BIT14,SSWREG      ; CHECK FOR LOOP ON ERROR
        001776 001366      BNE      LP1         ; GO TO LOOP ERROR
        001780 012767 000001 176374      MOV      #1,SEFATAL
        001786 012767 000001 176364      MOV      #1,SEFCTY
        001792 005767 176402      TST      SSWREG      ; MOVE ERROR NUM TO MAILBOX
        001796 100401      BHI      IS          ; CHECK FOR HALT ON ERROR
        001802 000000      HALT                ; HALT IF SET
        001806 000000      ; <CANNOT ACCESS RCSR>

        001810 032767 002000 176370      IS:     BIT      @BIT10,SSWREG      ; CHECK FOR LOOP ON TEST
        001816 001345      BNE      TST1        ; GO TO LOOP ON TEST
        001822 012737 000006 000004      MOV      #6,204      ; RESTORE TIMEOUT VECTOR

; TEST ABILITY TO REFERENCE RECEIVER BUFFER WITHOUT TRAPPING
TST2:   001826 012767 000002 176334      MOV      #2,STESTN      ; MOVE TEST NUMBER TO MAILBOX
        001834 012737 002004 000004      LP2:    MOV      #25,204 ; SET TIME OUT VECTOR
        001842 005777 176426      TST      @RBUF      ; REFERENCE THE BUFFER
        001846 000416      BR        IS          ; GO TO NEXT TEST

        001850 032767 040000 176330      ZS:     BIT      @BIT14,SSWREG      ; CHECK FOR LOOP ON ERROR
        001856 001366      BNE      LP2         ; GO TO LOOP ERROR
        001862 012767 000002 176300      MOV      #2,SEFATAL
        001868 012767 000001 176270      MOV      #1,SEFCTY
        001874 005767 176306      TST      SSWREG      ; MOVE ERROR NUM TO MAILBOX
        001878 100401      BHI      IS          ; CHECK FOR HALT ON ERROR
        001884 000000      HALT                ; HALT IF SET
        001888 000000      ; <CANNOT ACCESS RBUF>

        001892 032767 002000 176274      IS:     BIT      @BIT10,SSWREG      ; CHECK FOR LOOP ON TEST
        001898 001345      BNE      TST2        ; GO TO LOOP ON TEST
        001904 012737 000006 000004      MOV      #6,204      ; RESTORE TIMEOUT VECTOR

; TEST ABILITY TO REFERENCE TRANSMITTER CSR WITHOUT TRAPPING
TST3:   001908 012767 000003 176240      MOV      #3,STESTN      ; MOVE TEST NUMBER TO MAILBOX

```

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 DIVKREB.P11 ERROR 2 CANNOT ACCESS RBUF

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663 002144 012737 002160 000004 LP3: MOV 025,204 ;SET UP TIME OUT VECTOR
664 002151 005777 176334 TST ;REFERENCE THE T CSR
665 002158 000416 BR IS ;GO TO NEXT TEST IF NO TIME-OUT
666 002165 032767 040000 176234 25: BIT 0BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
667 002172 001366 LP3 ; GO TO LOOP ERROR
668 002179 012767 000003 176204 MOV 03,SEFATAL
669 002186 012767 000001 176174 MOV 01,SSGCTY ; MOVE ERROR NUM TO MAILBOX
670 002193 005767 176212 TST SSWREG ; CHECK FOR HALT ON ERROR
671 002200 100401 BHI IS ; HALT IF SET
672 002207 000000 HALT ;(<CANNOT ACCESS TCSR>)
673 002214 032767 002000 176200 15: BIT 0BIT10,SSWREG ; CHECK FOR LOOP ON TEST
674 002221 001366 TST3 ; GO TO LOOP ON TEST
675 002228 012737 000006 000004 MOV 06,204 ;RESTORE TIMEOUT VECTOR
676 002235 ;TEST ABILITY TO REFERENCE TRANSMITTER BUFFER WITHOUT TRAPPING
677 002242 TST4:
678 002249 012767 000004 176144 MOV 04,STESTN ; MOVE TEST NUMBER TO MAILBOX
679 002256 032767 000001 176152 BIT 0BIT0,SENV ; CHECK IF ON APT
680 002263 001406 LP4 ; DO THIS TEST IF NOT ON APT
681 002270 005767 176132 TST SPASS ; CHECK IF FIRST PASS
682 002277 001403 LP4 ; OR IF FIRST PASS
683 002284 005767 176222 TST CTSTFL ; IF NOT FIRST PASS - SKIP TEST
684 002291 001034 TST5 ; IF CONSOLE IS UNDER TEST
685 002298 012737 002300 000004 LP4: MOV 025,204 ;SET UP TIME-OUT VECTOR
686 002305 005777 176216 TST 0TBUF ;REFERENCE THE T BUFFER
687 002312 000416 BR IS ;GO TO NEXT TEST IF NO TIME-OUT
688 002319 032767 040000 176114 25: BIT 0BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
689 002326 001366 LP4 ; GO TO LOOP ERROR
690 002333 012767 000004 176054 MOV 04,SEFATAL
691 002340 012767 000001 176054 MOV 01,SSGCTY ; MOVE ERROR NUM TO MAILBOX
692 002347 005767 176072 TST SSWREG ; CHECK FOR HALT ON ERROR
693 002354 100401 BHI IS ; HALT IF SET
694 002361 000000 HALT ;(<CANNOT ACCESS TBUF>)
695 002368 032767 002000 176060 15: BIT 0BIT10,SSWREG ; CHECK FOR LOOP ON TEST
696 002375 001366 TST4 ; GO TO LOOP ON TEST
697 002382 012737 000006 000004 MOV 06,204 ;RESTORE TIMEOUT VECTOR
698 002389 NOP
699 002396 ;TEST THAT "BREAK" BIT (BIT0) IN TCSR CAN BE SET AND CLEARED AND
700 002403 ;THAT RESET CAN CLEAR IT.
701 002410 TST5:
702 002417 012767 000005 176022 MOV 05,STESTN ; MOVE TEST NUMBER TO MAILBOX
703 002424 032767 000001 176030 BIT 0BIT0,SENV ; CHECK IF ON APT
704 002431 001406 LP5A ; DO THIS TEST IF NOT ON APT
705 002438 005767 176010 TST SPASS ; CHECK IF FIRST PASS
706 002445 001403 LP5A ; OR IF FIRST PASS
707 002452 005767 176100 TST CTSTFL ; IF NOT FIRST PASS - SKIP TEST
708 002459 001136 TST6 ; IF CONSOLE IS UNDER TEST
709 002466 005004 LP5A: CLN R4 ; SET UP 300 MS COUNT
710 002473 005204 LP5B: INC R4
711 002480
712 002487
713 002494
714 002501
715 002508
716 002515
717 002522

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 DVKREB.P11 ERROR 4 CANNOT ACCESS TBUF

718	002412	001376			BNE	LPSB		
719	002414	000005			RESET			
720	002416	032777	000001	176066	BIT	ISBIT0, JTCSR		: CLEAR EVERYTHING
721	002424	001416			BEQ	TSCON		: CHECK BIT 0 (BREAK)
722	002426	032767	040000	175766	BIT	ISBIT14, SSMREG		: CONTINUE IF NOT SET
723	002434	001367			BNE	LPS		: CHECK FOR LOOP ON ERROR
724	002436	012767	000005	175736	MOV	85, SFATAL		: GO TO LOOP ERROR
725	002444	012767	000001	175726	MOV	81, MSGTY		: MOVE ERROR NUM TO MAILBOX
726	002452	005767	175744		TST	SSMREG		: CHECK FOR HALT ON ERROR
727	002460	100401			BMI	IS		: HALT IF SET
728	002462	000000			HALT			: <BIT 0 IN TCSR SHOULD BE 0 AFTER RESET>
729	002470	052777	000001	176022	IS:			
730	002472	032777	000001	176014	TSCON:	ISBIT0, JTCSR		: SET BIT0 (BREAK)
731	002474	001016			BIT	ISBIT0, JTCSR		: CHECK IF SET
732	002476	032767	040000	175714	BNE	TSCON1		: CONTINUE IF SET
733	002484	001365			BIT	ISBIT14, SSMREG		: CHECK FOR LOOP ON ERROR
734	002486	012767	000006	175644	BNE	TSCON		: GO TO LOOP ERROR
735	002488	012767	000001	175654	MOV	86, SFATAL		
736	002490	012767	000001	175654	MOV	81, MSGTY		: MOVE ERROR NUM TO MAILBOX
737	002492	005767	175672		TST	SSMREG		: CHECK FOR HALT ON ERROR
738	002494	100401			BMI	IS		: HALT IF SET
739	002496	000000			HALT			: <CANNOT SET BIT0 IN TCSR>
740	002504	042777	000001	175750	IS:			
741	002506	032777	000001	175742	TSCON1:	ISBIT0, JTCSR		: CLEAR BIT0
742	002508	001416			BIT	ISBIT0, JTCSR		: CHECK TO SEE IF CLEAR
743	002510	032767	040000	175642	BEQ	TSCON2		: CONTINUE IF CLEAR
744	002512	001365			BIT	ISBIT14, SSMREG		: CHECK FOR LOOP ON ERROR
745	002514	012767	000007	175612	BNE	TSCON1		: GO TO LOOP ERROR
746	002516	012767	000001	175602	MOV	87, SFATAL		
747	002518	012767	000001	175602	MOV	81, MSGTY		: MOVE ERROR NUM TO MAILBOX
748	002520	005767	175620		TST	SSMREG		: CHECK FOR HALT ON ERROR
749	002522	100401			BMI	IS		: HALT IF SET
750	002524	000000			HALT			: <CANNOT CLEAR BIT0 IN TCSR>
751	002532	012704	010000		IS:			
752	002534	005304			TSCON2:	810000, R4		: ; SET UP DELAY
753	002536	001376			TSEDEC:	R4		: ; DELAY
754	002538	052777	000001	175666	BNE	TSEDEC		
755	002540	000005			BIT	ISBIT0, JTCSR		: SET IT AGAIN
756	002542	032777	000001	175656	RESET	ISBIT0, JTCSR		: CHECK RESET CLEAR AGAIN
757	002544	001416			BIT	IS		: CHECK BIT 0
758	002546	032767	040000	175556	BEQ	ISBIT14, SSMREG		: CONTINUE IF RESET
759	002548	001360			BIT	TSCON2		: CHECK FOR LOOP ON ERROR
760	002550	012767	000010	175526	BNE	IS		: GO TO LOOP ERROR
761	002552	012767	000001	175516	MOV	810, SFATAL		
762	002554	005767	175534		MOV	81, MSGTY		: MOVE ERROR NUM TO MAILBOX
763	002556	100401			TST	SSMREG		: CHECK FOR HALT ON ERROR
764	002558	000000			BMI	IS		: HALT IF SET
765	002560				HALT			: <RESET DID NOT CLEAR BIT0 IN TCSR>
766	002562	032767	002000	175522	IS:			
767	002564	001225			BIT	ISBIT10, SSMREG		: CHECK FOR LOOP ON TEST
768	002566				BNE	TST5		: GO TO LOOP ON TEST

Address	Offset	Value	Label	Instruction	Comment
769					TEST THAT TCSR BIT6 (TRANSMITTER INTERRUPT ENABLE) CAN BE
770					SET AND RESET AND THAT RESET CLEARS IT.
771					
772					
773	002702	012767 000006 175474	TSTB:	MOV	%6,STESTN ; MOVE TEST NUMBER TO MAILBOX
774	002702	032767 000001 175502		BIT	BIT0,SENV ; CHECK IF ON APT
775	002710	001406		REQ	TST6A ; IF NOT ON APT
776	002716	001406		TST	SPASS ; CHECK IF ON FIRST PASS
777	002720	001406		REQ	TST6A ; BR, IF FIRST PASS
778	002724	001406		TST	CTSTFL ; IF NOT FIRST PASS - SKIP TEST
779	002726	001406		BNE	TST7 ; IF CONSOLE IS UNDER TEST
780	002732	001152			
781	002734	000005	TST6A:	RESET	SEND THE INITIAL RESET TO CLEAR
782	002734	012777 003014 175556	LP6:	MOV	ERR12,STVECT ; SET UP VECTOR IN CASE OF INTERRUPT
783	002736	105427 000200		HTPS	%200 ; TURN OFF INTERRUPTS
784	002744	032777 000100 175534		BIT	BIT6,STCSR ; CHECK IF BIT 6 IS ON
785	002750	001434		REQ	TCCON1 ; CONTINUE IF NOT SET
786	002756	032767 040000 175434		BIT	BIT14,SSMREG ; CHECK FOR LOOP ON ERROR
787	002760	001362		BNE	LP6 ; GO TO LOOP ERROR
788	002766	012767 000011 175404		MOV	%11,SPATAL ;
789	002770	012767 000001 175374		MOV	%1,MSGTY ; MOVE ERROR NUM TO MAILBOX
790	002776	005767 175412		TST	SSMREG ; CHECK FOR HALT ON ERROR
791	003004	100401		BMI	IS ; HALT IF SET
792	003010	000000		HALT	;<BIT6 IN TCSR NOT CLEAR AFTER RESET>
793	003012				
794	003014		IS:		
795	003014	032767 040000 175400	ERR12:	BIT	BIT14,SSMREG ; CHECK FOR LOOP ON ERROR
796	003022	001344		BNE	LP6 ; GO TO LOOP ERROR
797	003024	012767 000012 175350		MOV	%12,SPATAL ;
798	003030	012767 000001 175340		MOV	%1,MSGTY ; MOVE ERROR NUM TO MAILBOX
799	003040	005767 175366		TST	SSMREG ; CHECK FOR HALT ON ERROR
800	003044	100401		BMI	IS ; HALT IF SET
801	003046	000000		HALT	;<DEVICE SHOULD NOT HAVE INTERRUPTED WITH PRIORITY BIT SET>
802	003050		IS:		
803	003050	052777 000100 175434	TCCON1:	BIS	BIT6,STCSR ; SET BIT6
804	003052	032777 000100 175426		BIT	BIT6,STCSR ; CHECK IF SET
805	003064	001016		BNE	TCCON2 ; CONTINUE IF SET.
806	003066	032767 040000 175326		BIT	BIT14,SSMREG ; CHECK FOR LOOP ON ERROR
807	003074	001365		BNE	TCCON1 ; GO TO LOOP ERROR
808	003076	012767 000013 175276		MOV	%13,SPATAL ;
809	003104	012767 000001 175266		MOV	%1,MSGTY ; MOVE ERROR NUM TO MAILBOX
810	003112	005767 175304		TST	SSMREG ; CHECK FOR HALT ON ERROR
811	003116	100401		BMI	IS ; HALT IF SET
812	003120	000000		HALT	;<CANNOT SET BIT6 IN TCSR>
813	003122		IS:		
814	003122	042777 000100 175362	TCCON2:	BIC	BIT6,STCSR ; CLEAR BIT6
815	003124	032777 000100 175354		BIT	BIT6,STCSR ; CHECK IF CLEAR
816	003136	001416		REQ	TCCON3 ; CONTINUE IF CLEAR
817	003140	032767 040000 175254		BIT	BIT14,SSMREG ; CHECK FOR LOOP ON ERROR
818	003146	001365		BNE	TCCON2 ; GO TO LOOP ERROR
819	003150	012767 000014 175224		MOV	%14,SPATAL ;
820	003156	012767 000001 175214		MOV	%1,MSGTY ; MOVE ERROR NUM TO MAILBOX
821	003164	005767 175232		TST	SSMREG ; CHECK FOR HALT ON ERROR
822	003170	100401		BMI	IS ; HALT IF SET
823	003172	000000		HALT	;<CANNOT CLEAR BIT6 IN TCSR>

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 DVKREB.P11 ERROR 14 CANNOT CLEAR BIT6 IN TCSR

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003174 052777 000100 175310 18:
003174 000005 16CON3: BIS #BIT6,TCSR ; SET BIT6 AGAIN
003202 032777 000100 175300 RESET ; TRY RESET AGAIN
003204 001416 000100 175300 BIT #BIT6,TCSR ; CHECK TO SEE IF CLEAR
003212 032767 040000 175200 BEQ 18 ; CONTINUE IF CLEAR
003222 001364 000015 175150 BIT #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
003224 012767 000001 175140 BNE 16CON3 ; GO TO LOOP ERROR
003232 012767 000001 175156 MOV #15,SPATL ; MOVE ERROR NUM TO MAILBOX
003240 005767 175156 MOV #1,MSGTY ; CHECK FOR HALT ON ERROR
003244 100401 TST SSWREG ; HALT IF SET
003246 000000 BHI 18 ; <RESET DID NOT CLEAR BIT6 IN TCSR>
003250 032767 002000 175144 18: BIT #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
003250 001211 BNE TST6 ; GO TO LOOP ON TEST
003256

```


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 DVKREB.P11 ERROR 15 RESET DID NOT CLEAR BIT6 IN TCSR

TEST THAT RCSR BIT6 (RCVR INTERRUPT ENABLE) CAN BE SET AND
 CLEARED, AND THAT RESET CLEARS IT.

TST7:

```

MOV      87,STESTN      ; MOVE TEST NUMBER TO MAILBOX
BIT      8010,SENV      ; CHECK IF ON APT
BEQ      TST7A          ; IF NOT ON APT
TST      SPASS          ; CHECK IF IN FIRST PASS
BEQ      TST7A          ; IF NOT FIRST PASS
TST      CTSTFL         ; IF NOT FIRST PASS - SKIP TEST
BNE      TST10          ; IF CONSOLE IS UNDER TEST

```

TST7A:

```

LP8:     MTPS           8200      ; DISABLE INTERRUPTS
        RESET          ; CLEAR EVERYTHING
        BIT            8016,RCR   ; CHECK BIT6 FOR 0
        BEQ           TBCON1     ; CONTINUE IF RESET
        BIT            80114,SSMREG ; CHECK FOR LOOP ON ERROR
        BNE           LP8        ; GO TO LOOP ERROR
        MOV           816,SEFATAL ; MOVE ERROR NUM TO MAILBOX
        MOV           81,MSGTY    ; CHECK FOR HALT ON ERROR
        TST           SSMREG      ; HALT IF SET
        BHI           IS         ; (BIT6 IN RCSR NOT CLEAR BY RESET)
        HALT

```

IS:

```

TBCON1:  BIS           8016,RCR   ; SET BIT6
        BIT            8016,RCR   ; CHECK IF BIT SET
        BNE           TBCON2     ; CONTINUE IF SET
        BIT            80114,SSMREG ; CHECK FOR LOOP ON ERROR
        BNE           TBCON1     ; GO TO LOOP ERROR
        MOV           817,SEFATAL ; MOVE ERROR NUM TO MAILBOX
        MOV           81,MSGTY    ; CHECK FOR HALT ON ERROR
        TST           SSMREG      ; HALT IF SET
        BHI           IS         ; (CANNOT SET BIT6 IN RCSR)
        HALT

```

IS:

```

TBCON2:  BIS           8016,RCR   ; CLEAR BIT6
        BIT            8016,RCR   ; CHECK IF CLEAR
        BEQ           TBCON3     ; CONTINUE IF RESET
        BIT            80114,SSMREG ; CHECK FOR LOOP ON ERROR
        BNE           TBCON2     ; GO TO LOOP ERROR
        MOV           820,SEFATAL ; MOVE ERROR NUM TO MAILBOX
        MOV           81,MSGTY    ; CHECK FOR HALT ON ERROR
        TST           SSMREG      ; HALT IF SET
        BHI           IS         ; (CANNOT CLEAR BIT6 IN RCSR)
        HALT

```

IS:

```

TBCON3:  BIS           8016,RCR   ; SET BIT6 AGAIN
        RESET          ; ISSUE ANOTHER RESET
        BIT            8016,RCR   ; CHECK IF RESET CLEARED BIT6.
        BEQ           IS         ; CONTINUE IF CLEAR
        BIT            80114,SSMREG ; CHECK FOR LOOP ON ERROR
        BNE           TBCON3     ; GO TO LOOP ERROR
        MOV           821,SEFATAL ; MOVE ERROR NUM TO MAILBOX
        MOV           81,MSGTY    ; CHECK FOR HALT ON ERROR
        TST           SSMREG

```

```

003260 012767 000007 175116
003260 032767 000001 175124
003266 001406
003274 005767 175104
003276 001403
003302 005767 175174
003304 001131
003310
003312 105427 000200
003316 000005
003320 032777 000100 175160
003326 001416
003330 032767 040000 175064
003336 001365
003340 012767 000016 175034
003346 012767 000001 175024
003354 005767 175042
003360 100401
003366 000000
003372 052777 000100 175114
003376 032777 000100 175106
003400 001016
003402 032767 040000 175012
003410 001365
003412 012767 000017 174762
003416 012767 000001 174752
003420 005767 174770
003426 100401
003430 000000
003436 042777 000100 175042
003440 032777 000100 175034
003446 001416
003450 032767 040000 174740
003456 001365
003460 012767 000020 174710
003464 012767 000001 174700
003470 005767 174716
003476 100401
003480 000000
003486 052777 000100 174770
003490 000005
003496 032777 000100 174760
003500 001416
003504 032767 040000 174664
003508 001364
003512 012767 000021 174634
003516 012767 000001 174624
003520 005767 174642

```

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 DVKREB.P11 ERROR 21 SECOND RESET DID NOT CLEAR BIT6

```

897 003560 100401      BMI      IS      ; HALT IF SET
898 003562 000000      HALT      ; <SECOND RESET DID NOT CLEAR BIT6>
899 003564 000000      IS:      ;
900 003564 032767 002000 174630      BIT      @BIT10,SSWREG      ; CHECK FOR LOOP ON TEST
901 003572 001232      BNE      TST7      ; GO TO LOOP ON TEST
902
903      ; TEST THAT RCSR BIT7 (RCVR DONE) IS CLEAR (BY RESET) AND
904      ; CAN BE READ RELIABLY.
905
906      TST10:
907 003574 012767 000010 174602      MOV      @10,STESTN      ; MOVE TEST NUMBER TO MAILBOX
908 003574 000005      RESET      ; CLEAR EVERYTHING
909 003602 032777 030000 174674      BIT      @BIT,RCRCSR      ; CHECK IF BIT7 CLEAR.
910 003612 001416      BEQ      IS      ; CONTINUE IF RESET
911 003614 032767 040000 174600      BIT      @BIT14,SSWREG      ; CHECK FOR LOOP ON ERROR
912 003622 001367      BNE      LP9      ; GO TO LOOP ERROR
913 003624 012767 000022 174550      MOV      @22,SFATAL
914 003632 012767 000001 174540      MOV      @1,MSGTY      ; MOVE ERROR NUM TO MAILBOX
915 003640 005767 174556      TST      SSWREG      ; CHECK FOR HALT ON ERROR
916 003644 100401      BMI      IS      ; HALT IF SET
917 003646 000000      HALT      ; <BIT7 IN RCSR NOT CLEAR BY RESET>
918
919      IS:
920 003650 032767 002000 174544      BIT      @BIT10,SSWREG      ; CHECK FOR LOOP ON TEST
921 003656 001346      BNE      TST10      ; GO TO LOOP ON TEST
922
923      ; TEST THAT RCSR BIT15 (DATA SET STATUS) IS CLEAR (BY RESET)
924      ; AND CAN BE READ RELIABLY.
925
926      TST11:
927 003660 012767 000011 174516      MOV      @11,STESTN      ; MOVE TEST NUMBER TO MAILBOX
928 003660 000005      RESET      ; CLEAR EVERYTHING
929 003662 032777 100000 174610      BIT      @BIT15,RCRCSR      ; CHECK IF BIT15 IS CLEAR
930 003670 001416      BEQ      IS      ; CONTINUE IF CLEAR
931 003672 032767 040000 174514      BIT      @BIT14,SSWREG      ; CHECK FOR LOOP ON ERROR
932 003706 001367      BNE      LP10      ; GO TO LOOP ERROR
933 003710 012767 000023 174464      MOV      @23,SFATAL
934 003716 012767 000001 174454      MOV      @1,MSGTY      ; MOVE ERROR NUM TO MAILBOX
935 003724 005767 174472      TST      SSWREG      ; CHECK FOR HALT ON ERROR
936 003730 100401      BMI      IS      ; HALT IF SET
937 003732 000000      HALT      ; <BIT15 IN RCSR NOT CLEAR BY RESET>
938
939      IS:
940 003734 032767 002000 174460      BIT      @BIT10,SSWREG      ; CHECK FOR LOOP ON TEST
941 003742 001346      BNE      TST11      ; GO TO LOOP ON TEST

```

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 DVKAEB.P11 ERROR 23 BIT15 IN RCSR NOT CLEAR BY RESET

TEST THAT LOADING TBUF CLEARS TCSR BIT7 (READY) AND THAT
 BIT7 IS SET AFTER THE TRANSMITTER IS DONE.

TST12:

```

MOV      R12,STESTN      ; MOVE TEST NUMBER TO MAILBOX
BIT      R10,SENV        ; CHECK IF ON APT
BEQ      NOAPT           ; IF NOT
TST      SPASS           ; CHECK IF IN FIRST PASS
BEQ      NOAPT           ; OR IF NOT FIRST PASS
TST      CTSFL          ; IF NOT FIRST PASS - SKIP TEST
BNE      TST13          ; IF CONSOLE IS UNDER TEST

```

NOAPT:

```

LP11:    RESET          ; INITIALIZE (SET TCSR BIT7)
        CLR      TBUF    ; MOVE ZEROS TO TBUFFER
        BIT      R17,TCSR ; CHECK IF BIT7 CLEAR.
        BEQ      T30CN1  ; CONTINUE IF CLEAR
; DO IT ONE MORE TIME IN CASE REFRESH BOMBED THE FIRST TEST
        CLR      TBUF    ; DROP READY WITH THIS CHAR.
        BIT      R17,TCSR ; CHECK FOR READY LOW
        BEQ      T30CN1  ; THIS IS A REAL ERROR IF NOT 0
        BIT      R14,SSWREG ; CHECK FOR LOOP ON ERROR
        BNE      LP11    ; GO TO LOOP ERROR
        MOV      R24,SEFATAL
        MOV      R1,MSGTY ; MOVE ERROR NUM TO MAILBOX
        TST      SSWREG   ; CHECK FOR HALT ON ERROR
        BHI      IS      ; HALT IF SET
        ;(<TCSR BIT DID NOT CLEAR AFTER DATA XMIT>)

```

IS:

```

T30CN1:  CLR      R1      ; CLEAR COUNT REG.
        BIS      R1,R1    ; SET COUNT
        DEC      R1      ; DECREMENT COUNT
        BNE      DECR    ; CONTINUE IF NOT 0
        BIT      R17,TCSR ; CHECK IF READY IS BACK ON.
        BNE      IS      ; CONTINUE IF SET.
        BIT      R14,SSWREG ; CHECK FOR LOOP ON ERROR
        BNE      LP11    ; GO TO LOOP ERROR

```

```

        MOV      R25,SEFATAL
        MOV      R1,MSGTY ; MOVE ERROR NUM TO MAILBOX
        TST      SSWREG   ; CHECK FOR HALT ON ERROR
        BHI      IS      ; HALT IF SET
        ;(<TCSR BIT7 DID NOT SET AFTER XMIT>)

```

IS:

```

BIT      R10,SSWREG      ; CHECK FOR LOOP ON TEST
BNE      TST12          ; GO TO LOOP ON TEST

```

TEST THAT THE TRANSMITTER CAN INTERRUPT AT THE CORRECT VECTOR

TST13:

```

MOV      R13,STESTN      ; MOVE TEST NUMBER TO MAILBOX
BIT      R10,SENV        ; CHECK IF ON APT
BEQ      TST13A          ; IF NOT ON APT
TST      SPASS           ; CHECK IF FIRST PASS
BEQ      TST13A          ; OR, IF NOT FIRST PASS
TST      CTSFL          ; IF NOT FIRST PASS - SKIP TEST

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003744 012767 000012 174432
003744 032767 000001 174440
003752 001406
003760 005767 174420
003762 001403
003766 005767 174510
003770 001066
003774
003776 000005
003776 005077 174510
004000 032777 000200 174500
004004 001424
004012
004014 005077 174474
004020 032777 000200 174464
004026 001416
004030 032767 040000 174364
004036 001357
004040 012767 000024 174334
004046 012767 000001 174324
004054 005767 174342
004060 100401
004062 000000
004064 005001
004066 052701 010000
004072 005301
004074 001376
004076 032777 000200 174406
004104 001016
004106 032767 040000 174306
004114 001330
004116 012767 000025 174256
004124 012767 000001 174246
004126 005767 174264
004130 100401
004136 000000
004140
004146 032767 002000 174252
004150 001275
004152 012767 000013 174224
004160 032767 000001 174232
004166 001406
004170 005767 174212
004174 001403
004176 005767 174302

```

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 DVKAE8.P11 ERROR 25 TCSR BIT7 DID NOT SET AFTER XMIT

```

996 004202 001043      BNE      TST14      ; IF CONSOLE IS UNDER TEST
997 004204      TST13A:      ;
998 004204 042777 000100 174300 LP12: BIC      #BIT6,2TCSR ; DISABLE XMITTER INTERRUPT
999 004212 012777 004304 174302      MOV      #T31CN1,2TVECT ; SET VECTOR ADDRESS
1000 004220 005077 174300      CLR      2TPSM ; SET PSM FOR INTERRUPT
1001 004224 106427 000000      MTPS     #0 ; ALLOW INTERRUPTS
1002 004230 052777 000100 174254      BIS      #BIT6,2TCSR ; ENABLE INTERRUPTS
1003 004236 000240      NOP ; GIVE IT SOME TIME
1004 004240 032767 040000 174154      BIT      #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
1005 004246 001356      BNE      LP12 ; GO TO LOOP ERROR
1006 004250 012767 000026 174124      MOV      #26,2SFATAL
1007 004256 012767 000001 174114      MOV      #1,2MSGTY ; MOVE ERROR NUM TO MAILBOX
1008 004264 005767 174132      TST      SSWREG ; CHECK FOR HALT ON ERROR
1009 004270 100401      BHI ; HALT IF SET
1010 004272 000000      HALT ; <NO INTERRUPT FROM DEVICE>
1011 004274      IS:
1012 004274 032767 002000 174120      BIT      #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
1013 004302 001323      BNE      TST13 ; GO TO LOOP ON TEST
1014 004304 042777 000100 174200 T31CN1: BIC      #BIT6,2TCSR ; DISABLE INTERRUPT
1015
1016 ; TEST THAT TRANSMITTER DOES NOT INTERRUPT WHEN PSM DISABLES
1017
1018 004312      TST14:
1019 004312 012767 000014 174064      MOV      #14,2TESTN ; MOVE TEST NUMBER TO MAILBOX
1020 004320 032767 000001 174072      BIT      #BIT0,2ENV ; CHECK IF ON APT
1021 004326 001406      BEQ      TST14A ; IF NOT ON APT
1022 004330 005767 174052      TST      2PASS ; CHECK IF IN FIRST PASS
1023 004334 001403      BEQ      TST14A ; BR, IF NOT FIRST PASS
1024 004336 005767 174142      TST      C1STFL ; IF NOT FIRST PASS - SKIP TEST
1025 004342 001041      BNE      TST15 ; IF CONSOLE IS UNDER TEST
1026 004344
1027 004344 042777 000100 174140 TST14A: BIC      #BIT6,2TCSR ; CLEAR INT ENABLE
1028 004352 106427 000200      MTPS     #200 ; DISABLE INTERRUPTS
1029 004356 012777 004402 174136      MOV      #26,2TVECT ; VECTOR POINT TO ERROR
1030 004364 005077 174134      CLR      2TPSM ; CLEAR PSM FOR INTERRUPT
1031 004370 052777 000100 174114      BIS      #BIT6,2TCSR ; ENABLE INTERRUPTS
1032 004376 000240      NOP ; GIVE IT SOME TIME
1033 004400 000416      BR ; CONTINUE IF NO INTERRUPT.
1034 004402
1035 004402 032767 040000 174012 25: BIT      #BIT14,SSWREG ; CHECK FOR LOOP ON ERROR
1036 004410 001356      BNE      LP13 ; GO TO LOOP ERROR
1037 004412 012767 000027 173762      MOV      #27,2SFATAL
1038 004420 012767 000001 173752      MOV      #1,2MSGTY ; MOVE ERROR NUM TO MAILBOX
1039 004426 005767 173770      TST      SSWREG ; CHECK FOR HALT ON ERROR
1040 004432 100401      BHI ; HALT IF SET
1041 004434 000000      HALT ; <DEVICE GAVE INTERRUPT WITH PSM DISABLE>
1042 004436
1043 004436 032767 002000 173756 15: BIT      #BIT10,SSWREG ; CHECK FOR LOOP ON TEST
1044 004444 001322      BNE      TST14 ; GO TO LOOP ON TEST
1045
1046 ; TEST THAT XMITTER DOES NOT RE-INTERRUPT AFTER THE FIRST
1047 ; INTERRUPT IS SERVICED.
1048
1049 004446      TST15:
1050 004446 012767 000015 173730      MOV      #15,2TESTN ; MOVE TEST NUMBER TO MAILBOX
1051 004454 032767 000001 173736      BIT      #BIT0,2ENV ; CHECK IF ON APT

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 DVKAEB.P11 ERROR 27 DEVICE GAVE INTERRUPT WITH PSM DISABLE

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1052 004462 001406      BEQ      TST15A      ; IF NOT ON APT
1053 004464 005767 173716 TST      SPASS      ; CHECK IF IN FIRST PASS
1054 004470 001403      BEQ      TST15A      ; BR, IF FIRST PASS
1055 004472 005767 174006 TST      CTSTFL    ; IF NOT FIRST PASS - SKIP TEST
1056 004476 001066      BNE      TST16      ; IF CONSOLE IS UNDER TEST
1057 004500      TST15A:
1058 004500 042777 000100 174004 LP14: BIC      @BIT6,@TCR ; CLEAR INTERRUPT DISABLE
1059 004506 012777 004570 174006      MOV      @T33CN1,@TVECT ; SET UP VECTOR ADDRESS
1060 004514 005077 174004      CLR      @TPSM      ; PSM FOR VECTOR
1061 004520 106427 000000      MTPS      80      ; ALLOW INTERRUPTS
1062 004524 052777 000100 173760      BIS      @BIT6,@TCR ; ENABLE INTERRUPT
1063 004532 000240      NOP      ; TIME
1064 004534 032767 040000 173660      BIT      @BIT14,@SSREG ; CHECK FOR LOOP ON ERROR
1065 004542 001356      BNE      LP14      ; GO TO LOOP ERROR
1066 004544 012767 000030 173630      MOV      @30,@FATAL
1067 004552 012767 000001 173620      MOV      @1,@MSGTY ; MOVE ERROR NUM TO MAILBOX
1068 004560 005767 173636      TST      @SSREG      ; CHECK FOR HALT ON ERROR
1069 004564 100401      BHI      18      ; HALT IF SET
1070 004566 000000      HALT      ; <DEVICE FAILED TO INTERRUPT>
1071 004570      18:
1072 004570 012777 004610 173724 T33CN1: MOV      @ERR26,@TVECT ; SET UP VECTOR FOR RE-INTERRUPT
1073 004576 005016      CLR      (SP)
1074 004600 012746 004654      MOV      @TST16,-(SP) ; POINT TO NEXT TEST FOR RTI
1075 004604 000002      RTI
1076 004606 000240      NOP      ; SERVICE INTERRUPT
1077 004610      ERR26:
1078 004610 032767 040000 173604      BIT      @BIT14,@SSREG ; CHECK FOR LOOP ON ERROR
1079 004616 001364      BNE      T33CN1 ; GO TO LOOP ERROR
1080 004620 012767 000031 173554      MOV      @31,@FATAL
1081 004626 012767 000001 173544      MOV      @1,@MSGTY ; MOVE ERROR NUM TO MAILBOX
1082 004634 005767 173562      TST      @SSREG      ; CHECK FOR HALT ON ERROR
1083 004640 100401      BHI      18      ; HALT IF SET
1084 004642 000000      HALT      ; <DEVICE RE-INTERRUPTED AFTER FIRST INTERRUPT SERVICE>
1085 004644      18:
1086 004644 032767 002000 173550      BIT      @BIT10,@SSREG ; CHECK FOR LOOP ON TEST
1087 004652 001275      BNE      TST15      ; GO TO LOOP ON TEST
1088
1089      ; TEST TRANSMITTER AND RECIEVER BUFFERS.
1090      ; NOTE: SPECIAL WRAP MODULE MUST BE INSTALLED TO RUN
1091      ; THIS TEST. THIS TEST WILL RUN IF BIT9 OF SSREG =1.
1092
1093      TST16:
1094 004654 012767 000016 173522      MOV      @16,@TESTN ; MOVE TEST NUMBER TO MAILBOX
1095 004662 032767 000001 173530      BIT      @BIT0,@ENV ; CHECK IF ON APT
1096 004670 001406      BEQ      NOAPT1 ; IF NOT
1097 004672 005767 173510      TST      SPASS      ; CHECK IF IN FIRST PASS
1098 004676 001403      BEQ      NOAPT1 ; BR, IF FIRST PASS
1099 004700 005767 173600      TST      CTSTFL    ; IF NOT FIRST PASS - SKIP TEST
1100 004704 001147      BNE      TST999 ; IF CONSOLE IS UNDER TEST
1101 004706      NOAPT1:
1102 004706 032767 001000 173506      BIT      @BIT9,@SSREG ; CHECK IF THIS TEST IS ENABLED
1103 004714 001537      BEQ      TST17 ; SKIP IF NOT
1104 004716 000006      RESET ; CLEAR EVERYTHING
1105 004720 106427 000200      MTPS      8200 ; DISABLE INTERRUPTS
1106 004724 012703 000020      MOV      @20,@R3 ; SET SYNC COUNTER
1107 004730 005777 173554      TST      @RBUF ; CLEAR BUFFER

```

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 DVKAEB.P11 ERROR 31 DEVICE RE-INTERRUPTED AFTER FIRST INTERRUPT SERVICE

1108	004734	005004			CLR	R4	:	CLEAR DELAY COUNTER
1109	004736	005204			INC	R4	:	DELAY 300 MS
1110	004740	001376			BNE	INCR4	:	
1111	004742	052777	000011	173536	BITS	#11,ARCSR	:	SET READER ENABLE
1112	004750	000240			NOP		:	
1113	004752	000240			NOP		:	
1114	004754	105777	173532		CHK1: TSTB	ATCSR	:	CHECK FOR XMITTER DONE
1115	004760	100375			BPL	CHK1	:	WAIT TIL READY
1116	004762	012777	000125	173524	MOV	#125,ATBUF	:	SEND DATA
1117	004770	105777	173512		CHK2: TSTB	ARCSR	:	WAIT FOR RCVR DONE
1118	004774	100375			BPL	CHK2	:	
1119	004776	122777	000125	173504	CHKSYN: CNPB	#125,ARBUF	:	CHECK FOR SYNC BYTE
1120	005004	001426			BQA	T34CON	:	CONTINUE IF FOUND
1121	005006	005303			DEC	R3	:	DECREMENT SYNC COUNTER
1122	005010	001367			BNE	CHK2	:	CONTINUE TIL SYNC UP
1123	005012	012777	000001	173466	MOV	#BIT0,ARCSR	:	TURN OFF WRAP MODULE
1124	005014	000240			NOP		:	
1125	005016	000240			NOP		:	
1126	005018	000005			RESET		:	
1127	005020	032767	040000	173366	BIT	#BIT14,SSWREG	:	CHECK FOR LOOP ON ERROR
1128	005022	001330			BNE	LP15	:	GO TO LOOP ERROR
1129	005024	012767	000032	173336	MOV	#32,SFATAL	:	
1130	005026	012767	000001	173326	MOV	#1,MSGTY	:	MOVE ERROR NUM TO MAILBOX
1131	005028	005767	173344		TST	SSWREG	:	CHECK FOR HALT ON ERROR
1132	005030	100401			BMI	IS	:	HALT IF SET
1133	005032	000000			HALT		:	<CANNOT GET TEST MODULE IN SYNC>
1134	005034	005001			IS: T34CON: CLR	R1	:	INITIALIZE DATA REG
1135	005036	012702	177777		MOV	#-1,R2	:	INITIALIZE R2
1136	005038	005777	173414		TST	ARBUF	:	FORCE BUFFER CLEAR
1137	005040	105777	173412		CHKT: TSTB	ATCSR	:	CHECK XMITTER DONE
1138	005042	100375			BPL	CHKT	:	WAIT TIL DONE
1139	005044	010177	173406		SDATA: MOV	R1,ATBUF	:	SEND DATA
1140	005046	105777	173374		CHKR: TSTB	ARCSR	:	CHECK FOR RCVR DONE
1141	005048	100375			BPL	CHKR	:	WAIT TIL DONE
1142	005050	017702	173370		MOV	ARBUF,R2	:	GET WRAPPED DATA
1143	005052	020102			CNP	R1,R2	:	CHECK DATA
1144	005054	001012			BNE	R3	:	
1145	005056	005201			INC	R1	:	INCREMENT DATA
1146	005058	105701			TSTB	R1	:	CHECK FOR END OF DATA
1147	005060	001364			BNE	SDATA	:	CONTINUE LOOP
1148	005062	012777	000001	173346	MOV	#BIT0,ARCSR	:	TURN OFF LOOP
1149	005064	000240			NOP		:	
1150	005066	000240			NOP		:	
1151	005068	000005			RESET		:	
1152	005070	000422			BR		:	
1153	005072	032767	040000	173244	28: BIT	#BIT14,SSWREG	:	CHECK FOR LOOP ON ERROR
1154	005074	001353			BNE	CHKR	:	GO TO LOOP ERROR
1155	005076	012767	000033	173214	MOV	#33,SFATAL	:	
1156	005078	012767	000001	173204	MOV	#1,MSGTY	:	MOVE ERROR NUM TO MAILBOX
1157	005080	005767	173222		TST	SSWREG	:	CHECK FOR HALT ON ERROR
1158	005082	100401			BMI	IS	:	HALT IF SET
1159	005084	000000			HALT		:	<DATA DID NOT COMPARE ON SLU WRAP>
1160	005086	032767	002000	173210	IS: BIT	#BIT10,SSWREG	:	CHECK FOR LOOP ON TEST

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 DVKARB.P11 ERROR 33 DATA DID NOT COMPARE ON SLU WRAP

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1164 005212 001220          BNE      TST16          ; GO TO LOOP ON TEST
1165 005213 000005          TST17:      RESET
1166 005214 005004          CLR      R4
1167 005215 005004          T35DEC:    DEC      R4          ; DEC TIMER
1168 005216 001376          BNE      T35DEC
1169 005217 005267 173160          TST999:    INC      SDEVCT          ; INC DEVICE COUNTER
1170 005218 026767 173244 173152 T999A:    CMP      TMP2, SDEVCT          ; ALL DEVICES TESTED?
1171 005219 001404          BEQ      T999B          ; IF YES
1172 005220 005067 173240          CLR      CISTFL          ; CLEAR CONSOLE UNDER TEST FLAG
1173 005221 000167 174360          JMP      SETUP          ; GO TEST NEXT DEVICE
1174 005222 005237 000406          T999B:    INC      PASS          ; INCREMENT PASS COUNT
1175 005223 004767 000046          JSR      PC, MSGPRT          ; PRINT END OF PASS
1176 005224 005572          .WORD
1177 005225 013700 000042          ACT:      MOV      @R4, R0          ; CHECK ACT
1178 005226 001405          BEQ      GOAGIN          ; KEEP GOING
1179 005227 000006          RESET
1180 005228 004710          SENDAD:    JSR      PC, (R0)          ; ACT HOOKS
1181 005229 000240          NOP
1182 005230 000240          NOP
1183 005231 000240          NOP
1184 005232 005067 173102          GOAGIN:    CLR      SDEVCT          ; RESET DEVICE COUNT
1185 005233 022767 000001 173164      CMP      #1, TMP2          ; IS THIS THE ONLY DEVICE UNDER TEST?
1186 005234 001026          BNE      RSTRT          ; IF NO
1187 005235 001270 001000          MOV      #STKPTR, SP          ; INITIALIZE STACK POINTER
1188 005236 000167 174420          JMP      TST1          ; GO DO ANOTHER PASS
1189 005237 132767 000040 173065      MSGPRT:    BITB      #40, SENVM          ; WILL APT ALLOW PRINTING?
1190 005238 001403          BEQ      TYPE          ; YES
1191 005239 062716 000002          ADD      #2, (SP)          ; ADJUST RETURN
1192 005240 000207          RTS      PC          ; RETURN
1193 005241 011600          TYPE:      MOV      (SP), R0          ; GET MESSAGE ADDRESS
1194 005242 011000          WAIT:      MOV      (R0), R0          ; GET READY TO PRINT
1195 005243 105777 000030          TSTB      #TPS          ; CHECK IF TTY READY
1196 005244 100375          BPL      WAIT          ; IF NOT
1197 005245 112077 000020          MOVB      (R0), #TPB          ; PRINT THE CHARACTER
1198 005246 001372          BNE      WAIT          ; NEXT IF NOT DONE
1199 005247 062716 000002          ADD      #2, (SP)          ; ADJUST RETURN
1200 005248 000207          RTS      PC          ; RETURN
1201 005249 005067 173014          RSTRT:    CLR      SUNIT          ; START OVER
1202 005250 000167 173576          JMP      START
1203 005251 177566          .WORD 177566
1204 005252 177564          .WORD 177564
1205 005253 000000          ENDTST: 0
1206 005254 000000          UINT:
1207 005255 012767 000034 172764          NOV      #34, SFATAL          ; MOVE ERROR NUM TO MAILBOX
1208 005256 012767 000001 172754          NOV      #1, MSGTY          ; (UNEXPECTED INTERRUPT)
1209 005257 000000          HALT
1210 005258 000000          IS:
1211 005259 012737 005446 000024      PWRFL:    NOV      #PWRUP, #24          ; SET POWER UP VECTOR
1212 005260 012737 000340 000026          NOV      #340, #26          ; SET POWER UP PSM
1213 005261 000000          HALT
1214 005262 000776          BR

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 DVKAE.B.P11 ERROR 34 UNEXPECTED INTERRUPT

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1220
1221 005446 012737 005426 000024 PWRUP: MOV @PWRFL,2824 ;SET POWER FAIL VECTOR
1222 005454 005037 000026 CLR 2826 ;SET POWER UP PSM
1223 005460 005000 CLR R0 ;CLEAR TTY WAIT TIMER
1224 005462 005200 TTYWT: INC R0 ;INCREMENT TIMER
1225 005464 001376 BNE TTYWT ;WAIT FOR TTY POWER UP
1226 005466 C 4767 177634 JSR PC,HSGPRT ;TYPE "POWER" MESSAGE
1227 005472 005610 .WORD M4
1228 005474 000167 172520 JNP PRCONT ;START AT BEGINNING OF PRESENT PASS
1229
1230 005500 040515 047111 042504 M1: .ASCIZ .MAINDEC-11-DVKA-E-B DLVII TEST.<15><12>
1231 005506 026503 030461 042055
1232 005514 045526 042501 041055
1233 005522 020040 042011 053114
1234 005530 044511 052040 051505
1235 005536 006524 000012
1236 005542 020040 042040 053105 M2: .ASCIZ . DEVICES UNDER TEST.<15><12>
1237 005550 041511 051505 052440
1238 005556 042116 051105 052040
1239 005564 051505 006524 000012
1240 005572 047105 020104 043117 M3: .ASCIZ .END OF PASS.<15><12>
1241 005600 050040 051501 006523
1242 005606 000012
1243 005610 047520 042527 006522 M4: .ASCIZ .POWER.<15><12>
1244 005616 000012 .END
1245 000001
  
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.MAIN. MACY11 27(732) 04-OCT-76 14:23 PAGE 32
 DVKREB.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

TST1	001746	53	618	6218	636	1191												
TST10	0013574	906	906	920														
TST11	0013566	939	939															
TST12	0013741	985	985															
TST13	0014150	994	994	1013														
TST13B	0014150	994	994	997														
TST14	0014312	1018	1018	1044														
TST14B	0014344	1023	1023	1026														
TST15	0014446	1049	1049	1087														
TST15B	0014500	1054	1054	1057														
TST16	0014510	1074	1074	1093	1164													
TST17	0015214	1153	1153	1165														
TST2	0015204	655	655															
TST3	0015213	675	675															
TST4	0015213	680	680															
TST5	0015213	687	687	768														
TST6	0015270	715	715	773														
TST6A	0015274	776	776	778														
TST7	0015280	780	780	845														
TST7A	0015312	848	848	850														
TST999	0015312	850	850	853														
TIYMI	0015312	1100	1100	1170														
TVECT	0015312	1224	1224	1225														
TYPE	0015312	477	477	783	999	1029	1059	1072										
T30CN1	0015312	1193	1193	1196														
T31CN1	0015312	957	957	961	970													
T33CN1	0015312	999	999	1014														
T34CON	0015312	1059	1059	1072	1079													
T35DEC	0015312	1120	1120	1135														
TECON	0015312	1168	1168	1169														
TECON1	0015312	721	721	730	734													
TECON2	0015312	732	732	741	745													
TEDEC	0015312	743	743	752	760													
TECON1	0015312	753	753	754														
TECON2	0015312	754	754	804	808													
TECON3	0015312	805	805	815	819													
TECON1	0015312	817	817	825	831													
TECON2	0015312	857	857	865	870													
TECON3	0015312	858	858	877	881													
T999A	0015312	879	879	888	893													
T999B	0015312	1172	1172	1176														
UINT	0015312	1173	1173															
VCTROR	0015312	1204	1204															
VCTTBL	0015312	527	527	552														
VECT	0015312	443	443	613														
MAIT	0015312	614	614	617														
X	000017	1198	1198	1199	1201													
		439	439	622	623	641	642	661	662	681	682	709	710	774	775			
		847	847	907	907	908	926	927	945	946	990	991	1019	1020	1050			
		1051	1051	1094	1095													
SAPTHD	000460	423	423	429	520	532												
BASE	000460	410	410	513														
FLUP	000460	384	384															
DEVCT	000460	360	360	375	1171	1172	1186											
DEVH	000460	411	411	511	517	519	525	543	584	595								
ENDRD	000460	1182	1182															
ENDV	000460	380	380	501	682	710	775	847	946	991	1020	1051	1095					

SENVN	000421	381#	503	1192												
SETAB	000420	379#														
SETEND	000460	412#	435													
SFATAL	000402	358#	372#	629#	648#	668#	694#	724#	735#	746#	761#	789#	798#	809#		
		820#	832#	850#	871#	882#	894#	913#	932#	964#	978#	1006#	1037#	1066#		
		1080#	1129#	1157#	1210#											
SHIBTS	000460	430#														
SHADR1	000432	397#														
SHADR2	000433	401#														
SHADR3	000442	404#														
SHADR4	000446	407#														
SHAIL	000400	370#	431	435												
SHAPS1	000430	391#														
SHAPS2	000434	394#														
SHAPS3	000440	402#														
SHAPS4	000444	405#														
SHRDR	000462	431#														
SHSGAD	000414	377#														
SHSGLG	000416	378#														
SHSGTY	000400	371#	630#	649#	669#	695#	725#	736#	747#	762#	790#	799#	810#	821#		
		833#	861#	872#	883#	895#	914#	933#	965#	979#	1007#	1038#	1067#	1081#		
		1130#	1158#	1211#												
SHYTP1	000431	392#														
SHYTP2	000435	400#														
SHYTP3	000441	403#														
SHYTP4	000445	406#														
SPASS	000406	357#	374#	499	684	712	777	849	948	993	1022	1053	1097	1176#		
SPASTH	000461	433#														
SPAREC	000422	382#	505	627	631	635	646	650	654	666	670	674	692	696		
		722#	726	726	733	737	744	748	759	763	767	787	791	796		
		807#	811	810	822	830	834	838	858	862	869	873	880	880		
		892#	896	900	911	915	919	930	934	938	962	966	976	976		
		984#	1004	1008	1012	1035	1039	1043	1064	1068	1078	1082	1086			
		1102#	1127	1131	1155	1159	1163									
STESTN	000404	359#	373#	622#	641#	661#	681#	709#	774#	846#	907#	926#	945#	990#		
		1019#	1050#	1094#												
STSTN	000464	432#														
SUNIT	000412	361#	376#	599#	601#	1204#										
SUNITH	000470	434#														
SUSAR	000424	383#														
SVECT1	000460	438#	554													
SVECT2	000452	439#														
.	= 005620	318#	320	322	324	326	328	330#	331	333	335	337#	338	340		
		342#	344	346	348	351#	354#	355#	419	420#	422#	424#	441#	492#		
		493#	494#	1218												
.BX	= 000460	419#	424													

[illegible]

..S9902	10	
..S9903	10	
..S9904	10	
..S9905	10	
..S9906	10	
..S9907	10	
..S9908	10	
..S9909	10	
..S9910	10	
..S9911	10	
..S9912	10	
..S9913	10	
..S9914	10	
..S9915	10	
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..S9926	10	
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..S9930	10	
..S9931	10	
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..S9936	10	
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..S9938	10	
..S9939	10	
..S9940	10	
..S9941	10	
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..S9968	10	
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..S9971	10	
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..S9982	10	
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..S9986	10	
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..S9988	10	
..S9989	10	
..S9990	10	
..S9991	10	
..S9992	10	
..S9993	10	
..S9994	10	
..S9995	10	
..S9996	10	
..S9997	10	
..S9998	10	
..S9999	10	
..S10000	10	
..S10001	10	
..S10002	10	
..S10003	10	
..S10004	10	
..S10005	10	
..S10006	10	
..S10007	10	
..S10008	10	
..S10009	10	
..S10010	10	
..S10011	10	
..S10012	10	
..S10013	10	
..S10014	10	
..S10015	10	
..S10016	10	
..S10017	10	
..S10018	10	
..S10019	10	
..S10020	10	
..S10021	10	
..S10022	10	
..S10023	10	
..S10024	10	
..S10025	10	
..S10026	10	
..S10027	10	
..S10028	10	

840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	-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.MAIN. MACY11 27(732) 04-OCT-76 14:23 PAGE 39
 DVKAEB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

TSTB	1114	1117	1138	1141	1147	1198											
.ASCIZ	1230	1236	1240	1243													
.BLK	493	493															
.BYTE	360	381	391	392	399	400	402	403	405	406							
.ENABL		316															
.END	1234																
.ENDC	1234																
	1234	391	399	405	408	409	410	411	414	417	419	426	629	633			
	1234	746	752	761	762	766	769	793	795	798	802	804	809	813			
	1234	820	824	832	836	840	860	864	866	871	875	877	882	886			
	1234	941	944	913	917	921	932	936	940	964	968	970	978	982			
	1234	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1088	1129	1133			
	1234	1157	1161	1165	1210	1212	1214										
.EVEN																	
.IF																	
	1234	391	399	405	408	409	410	411	412	414	416	418	425	627			
	1234	746	752	761	762	766	769	793	795	798	802	804	809	813			
	1234	820	824	832	836	840	860	864	866	871	875	877	882	886			
	1234	941	944	913	917	921	932	936	940	964	968	970	978	982			
	1234	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1088	1129	1133			
	1234	1157	1161	1165	1210	1212	1214										
.IFF																	
.IFF																	
.LIST																	
	1234	318	369	623	629	630	642	648	649	662	668	669	692	694	695		
	1234	746	752	761	762	766	769	793	795	798	802	804	809	813			
	1234	820	824	832	836	840	860	864	866	871	875	877	882	886			
	1234	941	944	913	917	921	932	936	940	964	968	970	978	982			
	1234	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1088	1129	1133			
	1234	1157	1161	1165	1210	1212	1214										
.MACRO																	
.MCALL																	
.NEXT																	
.NLIST																	
	1234	317	369	623	629	630	642	648	649	662	668	669	692	694	695		
	1234	746	752	761	762	766	769	793	795	798	802	804	809	813			
	1234	820	824	832	836	840	860	864	866	871	875	877	882	886			
	1234	941	944	913	917	921	932	936	940	964	968	970	978	982			
	1234	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1088	1129	1133			
	1234	1157	1161	1165	1210	1212	1214										
.PAGE																	
.REH																	
.REPT																	
.SETTL																	
	1234	414	629	648	668	694	724	735	746	761	789	798	809	820	832		
	1234	941	944	913	917	921	932	936	940	964	968	970	978	982			
	1234	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1088	1129	1133			
	1234	1157	1161	1165	1210	1212	1214										
.WORD																	
	1234	414	629	648	668	694	724	735	746	761	789	798	809	820	832		
	1234	941	944	913	917	921	932	936	940	964	968	970	978	982			
	1234	1006	1010	1014	1037	1041	1045	1066	1070	1072	1080	1088	1129	1133			
	1234	1157	1161	1165	1210	1212	1214										

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

#, DVKAEB, SEQ/SOL/CRF/PAGNUM/NL: TOC=SYSHAC.CO, DVKAEB.P11
 RUN-TIME: 24 28 2 SECONDS
 RUN-TIME RATIO: 217/56=3.8
 CORE USED: 33K (65 PAGES)